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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,347	10/21/2003	Tiemin Zhao	38493-8017US1	6636
25096	7590	05/14/2007		
PERKINS COIE LLP PATENT-SEA P.O. BOX 1247 SEATTLE, WA 98111-1247			EXAMINER TRAN, NHAN T	
			ART UNIT 2622	PAPER NUMBER
			MAIL DATE 05/14/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/691,347	<b>Applicant(s)</b> ZHAO ET AL.	
	<b>Examiner</b> Nhan T. Tran	<b>Art Unit</b> 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 10/21/2003 & 2/4/2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,13-17,20-24 and 27-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,13-17,20-22,24,27-29 and 31 is/are rejected.
- 7) ☒ Claim(s) 23 and 30 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Information Disclosure Statement***

1. The information disclosure statements (IDS) submitted on 10/21/2003 & 2/4/2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

### ***Preliminary Amendments***

2. The preliminary amendment to specification filed on 10/21/2003 is accepted. The preliminary amendments filed 2/4/2004 including specification, drawings and claims are also accepted.

Currently, claims 1, 13-17, 20-24, 27-31 are pending. Claims 2-12, 18, 19, 25 & 26 have been canceled.

### ***Claim Objections***

3. Claim 1 is objected to because of the following informalities: claim 1 recites, "**the, selected critical level**" in line 9 of the claim. The comma (,) between "the" and "selected" should be removed. Appropriate correction is required.

### ***Double Patenting***

***(An Important Note: This application is a voluntary division of the parent application No. 09/461668 filed 12/14/1999, which is now US Patent No. 6,727,946. No restriction was made by the USPTO in the parent application. Thus, prohibition of double patenting rejections under 35 USC 121 does not apply. See MPEP 804.01.)***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 13-17, 20-24 & 27-31 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3-5 & 11-22 of U.S. Patent No. 6,727,946. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims 1, 13-17, 20-24, 27-31 of the instant application are broader in every aspect than the patent claims 1, 3-5 & 11-22, and are therefore obvious variants thereof.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 13-17, 20-22, 24, 27-29, 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US 6,111,245).

Regarding claim 1, Wu discloses an active pixel sensor circuit (Figs. 3-6), comprising:

- a sensor (D2) for producing a sensor potential;
- a pull-down circuit (M1, M3, M4 & M5) for implementing a pull down function during which the sensor potential is pulled down below a selected critical level (see Figs. 4 & 6 and col. 2, line 18 – col. 3, line 62);
- a reset voltage line (VDD) coupled to the pull-down circuit; and a reset transistor (M2) coupled between the reset voltage line and the sensor, wherein during the pull down function the reset transistor is conducting and the pulldown circuit operates to pull down the sensor potential below the, selected critical level, the pull down function being performed prior to the completion of a reset function when the sensor potential is reset to a selected level (see Figs. 4 & 6 and col. 2, line 18 – col. 3, line 62).

Regarding claim 13, it is clear in Wu that the sensor comprises a photodiode (D2).

Regarding claim 14, Wu discloses that the selected critical level is determined according to the potential at which the reset transistor will be on when the reset function starts (see col. 2, line 18 – col. 3, line 62).

Regarding claim 15, Wu also discloses that the timing of the pull down function is such that the sensor is stabilized at a level below the selected critical level before the reset function starts (see Figs. 4 & 6 and col. 2, line 18 – col. 3, line 62).

Regarding claims 16 & 17, these method claims are also met by the analyses of apparatus claims 1 & 15.

Regarding claim 20, as disclosed by Wu is that the sensor (D2) is coupled through a plurality of transistors (M1, M3) to a bit line (BL), and the bit line is used to pull down the sensor potential (see Figs. 3-6 and col. 2, line 18 – col. 3, line 62).

Regarding claim 21, it is seen in Fig. 3 of Wu that a loading transistor (M5) is coupled to the bit line (BL), and the voltage potential on the bit line is pulled down by increasing bias (by  $V_b$ ) on the loading transistor (col. 2, line 18 – col. 3, line 62).

Regarding claim 22, as shown in Fig. 3 of Wu, the gate of the loading transistor (M5) is coupled to a biasing circuit ( $V_b$ ), and the biasing circuit is used to increase the bias on the loading transistor (col. 2, line 18 – col. 3, line 62).

Regarding claim 24, Wu discloses an active pixel sensor circuit (Figs. 3-6) in which a soft reset function is performed, the active pixel sensor circuit comprising: a sensor (D2) which outputs a sensor potential; a reset transistor (M2) coupled to the sensor; a bit line (BL) coupled through a plurality of transistors (M1, M3 & M4) to the sensor, wherein the sensor potential is pulled below a selected critical level prior to the time when a soft reset function is performed to reset the sensor potential (col. 2, line 18 – col. 3, line 62).

Regarding claim 27, Wu further discloses that the bit line (BL) is used to pull the sensor potential below the selected critical level (col. 2, lines 18-57 and col. 3, lines 29-62).

Regarding claim 28, all limitations are met by the analysis of claim 21.

Regarding claim 29, also shown in Figs. 3-6, a biasing circuit (Vb) is coupled to the loading transistor (M5), the biasing circuit being used to increase the bias on the loading transistor so as to pull down the voltage level on the bit line (col. 2, line 18 – col. 3, line 62).

Regarding claim 31, Wu also discloses the selected critical level is determined according to the potential at which the reset transistor will be on when the soft reset function begins (col. 2, line 18 – col. 3, line 62).

***Allowable Subject Matter***

6. Claims 23 & 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims in addition to filing a **proper terminal disclaimer**.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

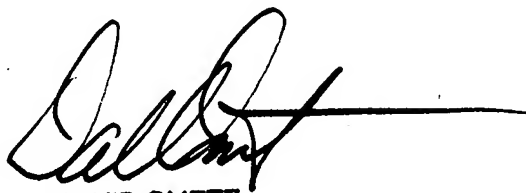
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN  
Patent Examiner

A handwritten signature in black ink, appearing to read 'David Ometz', with a long horizontal line extending to the right.

DAVID OMETZ  
SUPERVISORY PATENT EXAMINER